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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/583,883	05/31/2000	Terry R. Lee	M4065.0260/P260	1931

24998 7590 11/05/2004

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EXAMINER	
HUYNH, KIM T	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/583,883	LEE, TERRY R.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29 and 36-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29 and 36-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Affidavit, Exhibit

1. The Declaration of Terry R. Lee, Under 37CFR 1.131 filed 7/16/04 under 37 CFR 1.131 has been fully considered and has overcome in re Perino but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-14, 15-29, 36-44, 50-59, 65-68 are rejected under 35 U.S.C. 102(e) as being anticipated by Leddige et al. (US Patent 6,144,576)

As per claim 1, 14, Leddige discloses method of routing a system bus to a plurality of expansion cards said method comprises:

- routing the bus(fig.3, 300) into a first connector(fig.3, 220) and into a first circuit card (fig.3, 310) residing within the first connector; (col.3, lines 57-67)
- routing the bus from a portion of the first circuit card into a portion of a second circuit card residing within a second connector, wherein the bus is routed from the first circuit card to the second circuit card without entering the second connector; (col.3, line 57-col.4, 51)

- routing the bus through the second circuit card to the second connector. (col.4, lines 1-20)

As per claim 4, 17, Leddige discloses the method further comprising the act of routing the bus out of the second connector into a portion of a system circuit board. (col.4, lines 21-32)

As per claim 5, 18. Leddige discloses the method further comprising the act of terminating the bus after routing the bus out of the second connector. (col.4, lines 21-32)

As per claim 36, 51 Leddige discloses a bus system comprising:

- a bus (fig.3, 300) mounted on a circuit board of said system; (col.3, lines 57-67)
- a plurality of expansion slots, each slot comprising a connector mounted on said circuit board and a circuit card residing within the connector, wherein said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector and through said second circuit card, and wherein said bus is routed from said first circuit card to said second circuit card without entering said second connector. (col.2, lines 38-45), (col.3, line 57-col.4, line 51)

As per claims 2-3, 15-16, 37-38, 52-53 Leddige discloses the method further comprising the acts of routing bus into a third card (wherein bus routing 3rd to 4th

cards inherently disclose by method of bus routing from 1st to 2nd card as above.)

As per claims, 8, 21-22, 40 and 55, Leddige discloses wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a jumper mechanism. (col.5, lines 9-45), wherein printed wiring traces from 1st card to 2nd card implies jumper mechanism)

As per claim 6,7 and 19, 20, 42, 57 Leddige discloses the method wherein the first and second circuit cards each contain a top edge portion, each top edge portions being opposite an edge portion residing in a respective connector, arid wherein the bus is routed from the top edge portion of the first circuit card into the top edge portion of the second circuit card. (col.4, lines 33-51)

As per claim 9, 23, Leddige discloses wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a circuit board having bus portion traces for continuing the bus between the first and second circuit cards. (col.4, line 33-col.5, line 45)

As per claim 10, Leddige discloses wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a cable. (col.5, lines 9-45)

As per claim 11-13, 24-26 Leddige discloses wherein at least address, data and control signals are routed on said bus between the first and second circuit cards. (col.4, lines 52-60)

As per claim 27, Leddige discloses wherein the bus is routed into the first circuit card by routing the bus into a first connector in which the first circuit card is residing. (col.3, lines 57-67)

As per claim 28, Leddige discloses wherein the bus is routed out of the second circuit card by routing the bus out into a second connector in which the second circuit card is residing. (col.3, line 57-col.4, line 8)

As per claim 29, Leddige discloses wherein a first portion of bus signals are routed between the first and second circuit cards and a second portion of bus signals are provided to the second circuit card from the motherboard. (col.3, lines 35-56)

As per claim 34, Leddige discloses wherein the bus is routed to a first interface device connected the device on the first circuit card and the first interface device provides bus signals to the device on the first circuit card. (col.4, lines 52-60)

As per claim 35, Leddige discloses wherein the bus is routed to a second interface device connected the device on the second circuit card and the second interface device provides bus signals to the device on the second circuit card. (col.4, lines 52-60)

As per claim 39, 54 Leddige discloses wherein said bus is terminated by a plurality of resistors. (col.4, lines 22-32), wherein bus terminate inherently discloses resistors for each card)

As per claim 41, 56 Leddige discloses wherein said portions are located at a top edge of said first and second circuit cards opposite a bottom edge residing in said connectors. (col.5, lines 9-45)

As per claim 43, 58 Leddige discloses wherein said jumper mechanism comprises:

- a circuit board having bus portion traces configured for continuing said bus between said first and second circuit cards; (col.5, lines 9-45)
- a plurality of connectors coupled to said circuit board, at least one connector adapted to receive said portion of said first circuit card and at least one other connector adapted to receive. said portion of said second circuit card. (col.3, lines 35-56)

As per claim 44, 59, Leddige discloses wherein said jumper mechanism comprises:

- a cable configured for continuing said bus between said first and second circuit cards; (col.3, line 57-col.4, line 8)
- a plurality of connectors coupled to said cable, at least one connector adapted to receive said portion of said first circuit card and at least one other connector adapted to receive said portion of said second circuit card. (col.3, line 35-col.4, line 8)

As per claim 50, 65, Leddige discloses wherein said circuit cards are dynamic random access memory circuit cards and said system further comprises a memory controller coupled to said bus. (col.1, lines 13-19)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 45 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leddige et al. (US Patent 6,144,576) in view of Cargin, Jr. et al. (U.S Patent 6,023,147)

Leddige discloses the limitation of connection circuits via bus cable except Leddige fails to disclose specific type of cable as claimed in claims 45 and 60, the ribbon cable. However, Cargin discloses ribbon cable, (col.17, lines 21-29)
It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Cargin's teaching into Leddige's method to have a ribbon cable which the equivalent purpose of transmitting digital data between devices.

5. Claims 46-49 and 61-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leddige et al. (US Patent 6,144,576) in view of Handbook of LAN Cable Testing, Wavetek

Leddige discloses the limitation of connection circuits via bus cable except Leddige fails to disclose specific type of cable as claimed in claims 46-49 and 61-64,

ribbon cable with a shield , coaxial cable, a twisted pair wiring and a waveguide. However, the Handbook of Lan Cable Testing discloses different types of cable which included shied/unshield, coaxial cable, a twisted pair wiring and a waveguide. (see page 55-56)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate different types of cable into Leddige's method to have a variety of cable which the equivalent purpose of transmitting digital data between devices.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571)272-3632 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

Oct. 26, 2004

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100